ABSTRACT OF THE DISCLOSURE

In synchronization with a PLL clock PCK having a frequency four times that of an external clock ECK, n number of internal addresses IAD including an external address EAD are generated and, in synchronization with the PLL clock PCK, n bits of internal write data ITD are generated to be written into a RAM macro 12. Thereafter, the external address EAD is latched, n number of the internal addresses IAD including the external address EAD are generated in synchronization with the PLL clock PCK, n bits of internal read data ITQ corresponding to n number of the internal addresses IAD are read from the RAM macro 12 in synchronization with the PLL clock PCK and the internal read data ITQ corresponding to the internal address IAD which coincides with a latch address LAD among n number of the internal addresses IAD is outputted.